THAT WHICH IS CLAIMED IS:

1. An integrated circuit memory device, comprising:

a memory;

a read control circuit operatively associated with the memory and configured to produce data from the memory responsive to an externally applied input clock signal;

an output latch configured to transfer data at an input thereof to an output pad of the memory device responsive to an externally-applied output clock signal; and

a clock domain alignment circuit configured to receive the data produced by the memory and to responsively provide the data at the input of the output latch based on relative timing of the input clock signal and the output clock signal.

2. A device according to Claim 1, wherein the clock domain alignment circuit comprises:

a data input configured to receive the data produced by the memory;

a data latch having an input coupled to the data input and configured to transfer data to the input of the output latch and to hold data at the input of the output latch responsive to an alignment control signal;

a switch configured to couple the data input to the input of the output latch to bypass the data latch responsive to the alignment control signal; and

a control circuit that generates the alignment control signal responsive to the input clock signal and the output clock signal.

3. A device according to Claim 2, further comprising a delay locked loop circuit that generates an anticipatory clock signal that is synchronized with the externally-applied output clock signal, an output latch enable pulse generator that generates respective output latch enable pulses corresponding to respective edges of the anticipatory clock signal, wherein the output latch transfers data from its input to the external pin responsive to the output latch enable pulses, and wherein the control circuit comprises:

a first pulse generator that generates respective pulses corresponding to respective edges of the anticipatory clock signal;

a second pulse generator that generates respective pulses corresponding to respective edges of the input clock signal; and

a flip-flop that generates the alignment control signal responsive to the pulses generated by the first and second pulse generators.

4. A device according to Claim 3, wherein the second pulse generator is configured to suppress generation of pulses within a predetermined time interval with respect to pulses from the first pulse generator.

5. A device according to Claim 1, further comprising a delay locked loop circuit that generates an anticipatory clock signal that is synchronized with the output clock signal, wherein the output latch transfers data to the output pad responsive to the anticipatory clock signal, and wherein the clock domain alignment circuit is configured to drive the input of the output latch based on relative timing of the input clock signal and the anticipatory clock signal.

6. A device according to Claim 1, further comprising a read control circuit operative to initiate a read of the memory and to responsively produce a read cycle status signal, and wherein the clock domain alignment circuit transfers data to the output latch based on relative timing of the read cycle status signal and the output clock signal.

7. A device according to Claim 6, further comprising a delay locked loop circuit that generates an anticipatory clock signal that is synchronized with the externally-applied output clock signal, wherein the output latch transfers data responsive to the anticipatory clock signal, and wherein the clock domain alignment circuit comprises:

a clock domain alignment latch that receives data from the memory and transfers the data to the output latch responsive to a signal at a clock signal input thereof;

a data valid signal generator that generates a data valid signal indicative of the presence of valid data at an output of the memory responsive to the read cycle status signal;

a delay circuit that generates a delayed anticipatory clock signal from the anticipatory clock signal;

a latch that samples the data valid signal responsive to the delayed anticipatory clock signal to generate a select signal; and

a mux that selectively applies the data valid signal and the input clock signal to the clock signal input of the clock domain alignment latch.

8. An integrated circuit memory device, comprising:

a memory;

a memory interface circuit configured to receive a complementary input clock signal pair and a complementary output clock signal pair, operative to initiate reading of the memory synchronous with the input clock signal pair, and comprising an output latch configured to transfer read data at an input thereof to an output pad of the memory device responsive to the output clock signal pair; and

a clock domain alignment circuit configured to receive data from the memory and to selectively hold the data at the input of the output latch based on relative timing of the input clock signal pair and the output clock signal pair.

9. A device according to Claim 8, wherein the clock domain alignment circuit comprises:

a data input configured to receive the data produced by the memory;

a data latch having an input coupled to the data input and configured to transfer the data to the input of the output latch and to hold the data at the input of the output latch responsive to an alignment control signal;

a switch configured to couple the data input to the input of the output latch to bypass the data latch responsive to the alignment control signal; and

a control circuit that generates the alignment control signal responsive to one of the input clock signals and one of the output clock signals.

10. A device according to Claim 9, further comprising a delay locked loop circuit that generates an anticipatory clock signal that is synchronized with the output clock signal pair, an output latch enable pulse generator that generates respective output latch enable pulses corresponding to respective edges of the anticipatory clock signal, wherein the output latch transfers data from its input to the external pin responsive to the output latch enable pulses, and wherein the control circuit comprises:

a first pulse generator that generates respective pulses corresponding to respective edges of the anticipatory clock signal;

a second pulse generator that generates respective pulses corresponding to respective edges of one the input clock signals; and

a flip-flop that generates the alignment control signal responsive to the pulses generated by the first and second pulse generators.

11. A device according to Claim 10, wherein the second pulse generator is configured to suppress generation of pulses within a predetermined time interval with respect to pulses generated by the first pulse generator.

12. A device according to Claim 8, further comprising a delay locked loop circuit that generates an anticipatory clock signal that is synchronized with the output clock signal pair, wherein the output latch transfers data to the output pad responsive to the anticipatory clock signal, and wherein the clock domain alignment circuit is configured to drive the input of the output latch based on relative timing of the input clock signal pair and the anticipatory clock signal.

13. An integrated circuit memory device, comprising:

a memory; and

a memory interface circuit configured to receive a complementary input clock signal pair and a complementary output clock signal pair, operative to initiate reading of the memory synchronous with the input clock signal pair and to generate a read cycle status signal indicative of a status of a data read cycle of the memory, and comprising an output latch configured to transfer read data at an input thereof to an output pad of the memory device responsive to the output clock signal pair; and

a clock domain alignment circuit configured to transfer data to the input of the output latch based on relative timing of the read cycle status signal and the output clock signal pair.

14. A device according to Claim 13, further comprising a delay locked loop circuit that generates an anticipatory clock signal that is synchronized with the output clock signal pair, wherein the output latch transfers data responsive to the anticipatory clock signal, and wherein the clock domain alignment circuit comprises:

a clock domain alignment latch that receives data from the memory and transfers the data to the output latch responsive to a signal at a clock signal input thereof;

a data valid signal generator that generates a data valid signal indicative of the presence of valid data at an output of the memory;

a delay circuit that generates a delayed anticipatory clock signal from the anticipatory clock signal;

a latch that samples the data valid signal responsive to the delayed anticipatory clock signal to generate a select signal; and

a mux that selectively applies the data valid signal and one of the input clock signal pair to the clock signal input of the clock domain alignment latch responsive to the select signal.

15. A method of operating an integrated circuit memory device having a memory interface circuit configured to provide an input/output interface including an input clock signal pair and an output clock signal pair, the method comprising:

producing data from a memory of the device synchronous with the input clock signal pair;

selectively holding the data at the input of an output latch of the memory device based on relative timing of the input clock signal pair and the output clock signal pair; and

transferring data from the input of the output latch to an external pad of the memory device responsive to the output clock signal pair.

16. A method according to Claim 15, wherein selectively holding comprises:

generating an alignment control signal responsive to one of the input clock signals and one of the output clock signals;

receiving the data from the memory device at an input of a data latch and at a switch configured to couple the memory to the input of the output latch and operative to bypass the data latch; and

selectively holding data at the input of the output latch responsive to the alignment control signal or bypassing the data latch responsive to the alignment control signal.

17. A method according to Claim 16, wherein the memory device further comprises a delay locked loop circuit that generates an anticipatory clock signal that is synchronized with the output clock signal pair, wherein selectively holding comprises selectively holding the data at the input of an output latch of the memory device based on relative timing of one of the input clock signals and the anticipatory clock signal, and wherein transferring the data from the input of the output latch to an external pad of the memory device responsive to the output clock signal pair comprises transferring the data from the input of the output latch to the external pad responsive to the anticipatory clock signal.

18. A method according to Claim 17, wherein selectively holding the data at the input of an output latch of the memory device based on relative timing of the input clock signal pair and the anticipatory clock signal comprises:

generating an alignment control signal responsive to one of the input clock signals and the anticipatory clock signal;

receiving the data from the memory device at an input of a data latch and at a switch configured to couple the memory to the input of the output latch and operative to bypass the data latch; and

selectively holding data at the input of the output latch responsive to the alignment control signal or bypassing the data latch responsive to the alignment control signal.

19. A method of operating an integrated circuit memory device having a memory interface circuit configured to provide an input/output interface comprising a input clock signal pair and an output clock signal pair, the method comprising:

producing data from a memory of the device synchronous with the input clock signal pair;

transferring the data to an input of an output latch of the memory device based on relative timing of the output clock signal pair and a read cycle status signal indicative of a status of data read cycle of the memory; and

transferring data from the input of the output latch to an external pad of the memory device responsive to the output clock signal pair.

20. A method according to Claim 1, wherein the memory device further comprises a delay locked loop circuit that generates an anticipatory clock signal that is synchronized with the output clock signal pair, wherein the output latch transfers data responsive to the anticipatory clock signal, and wherein transferring the data comprises:

generating a data valid indicative of the presence of valid data at an output of the memory responsive to the read cycle status signal;

generating a delayed anticipatory clock signal from the anticipatory clock signal;

sampling the data valid signal responsive to the delayed anticipatory clock signal to generate a select signal; and

selecting one of the data valid signal or one of the input clock signals to apply to a clock signal input of a clock domain alignment latch responsive to the sampled data valid signal; and

transferring the data from the input of the clock domain alignment latch to the output latch responsive to the selected signal.